Electronic Version

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Claims

[c1] 1. A flip chip package structure, comprising:

a chip having a first bump-positioning region;

a substrate having a second bump-positioning region, at least a first hole and a plurality of second holes, wherein the first hole and the second holes are located within the second bump-positioning region, and the first hole has a depth greater than the second holes;

at least a first bump arranged between the first bump-positioning region of the chip and the second bump-positioning region of the substrate, wherein the first bump and the substrate are bonded together via the first hole; and

a plurality of second bumps arranged between the first bump-positioning region of the chip and the second bump-positioning region of the substrate, wherein the second bumps and the substrate are bonded together via the second holes;

wherein the first bump has a volume larger than avolume of the second bump.

[c2] 2. The flip chip package structure of claim 1, wherein when there is one first bump and one first hole, the first

bump is located in the middle of the first bump-positioning region of the chip and the first hole is located in the middle of the second bump-positioning region.

[c3] 3. The flip chip package structure of claim 1, wherein when there are two first bumps and two first holes, the two first bumps are positioned between the chip and the substrate and symmetrical relative to a centroid of the first bump-positioning region, and the two first holes are positioned in the second bump-positioning region and symmetrical relative to a centroid of the second bump-positioning region.

[c4] 4. The flip chip package structure of claim 1, wherein the package structure has a plurality of first bumps and the first bumps are located close to corners of the first bump-positioning region and located between the chip and the substrate, and the substrate has a plurality of first holes and the first holes are positioned close to corners of the second bump-positioning region.

[c5] 5. The flip chip package structure of claim 1, wherein the first bump arranged between the chip and the substrate physically but not electrically connects the chip and the substrate.

[c6] 6. The flip chip package structure of claim 1, wherein the first bump arranged between the chip and the substrate electrically and physically connects the chip and the substrate.

[c7] 7. The flip chip package structure of claim 1, further comprising a filler material disposed between the chip and the substrate and encapsulating the first bumps and the second bumps.

[c8] 8. A flip chip package structure, comprising:

a chip having a first bump-positioning region;

at least a first bump arranged within the first bump-positioning region; and

a plurality of second bumps arranged within the first bump-positioning region,

wherein the first bump has a configuration different from that of the second bump.

[c9] 9. The flip chip package structure of claim 8, wherein the first bump has a height greater than that of the second bump.

[c10] 10. The flip chip package structure of claim 8, wherein the package structure has one first bump positioned in the middle of the first bump-positioning region of the chip.

[c11] 11. The flip chip package structure of claim 8, wherein the package structure has two first bumps that are positioned on the first bump-positioning region of the chip and symmetrical relative to a centroid of the first bump-positioning region of the chip.

[c12] 12. The flip chip package structure of claim 8, wherein the package structure has a plurality of first bumps positioned close to corners of the first bump-positioning region of the chip.

[c13] 13. The flip chip package structure of claim 8, wherein the first bump arranged on the chip physically but not electrically connects the chip and the substrate.

[c14] 14. The flip chip package structure of claim 8, wherein the first bump arranged on the chip physically and electrically connects the chip and the substrate.

[c15] 15. The flip chip package structure of claim 8, wherein the first bump further comprises:
a conductive pillar arranged on the chip; and
a soldering block arranged on the conductive pillar.

[c16] 16. The flip chip package structure of claim 8, wherein the first bump has a height ranging from about 150μm to about 200μm.

[c17] 17. The flip chip package structure of claim 8, wherein the first bump has a volume greater than that of the second bump.

[c18] 18. A substrate having at least a first hole and a plurality of second holes positioned on a surface of the substrate, wherein the first hole has a depth greater than that of the second hole.

[c19] 19. The substrate of claim 18, wherein the substrate further comprises a plurality of electrical contacts exposed through the various second holes.

[c20] 20. The substrate of claim 18, wherein the substrate further comprises at least an electrical contact exposed through the first hole.

[c21] 21. The substrate of claim 18, wherein the substrate further has a bump-positioning region with one first hole positioned in the middle of the bump-positioning region.

[c22] 22. The substrate of claim 18, wherein the substrate further has a bump-positioning region with two first holes that are positioned in the bump-positioning region and symmetrical relative to a centroid of the bump-positioning region.

[c23] 23. The substrate of claim 18, wherein the substrate further has a bump-positioning region with a plurality of first holes positioned close to corners of the bump-positioning region.

[c24] 24. A method of joining carriers together, comprising the steps of:
providing a first carrier;
attaching at least a first bump and a plurality of second bumps to the first carrier, wherein the first bump has a structural configuration different from that of the second bump;
providing a second carrier, wherein the second carrier has a first hole and a plurality of second holes;
positioning the first carrier over the second carrier such that the first bump engages tightly with the first hole of the second carrier through a tight-fit mechanism and the second bumps are substantially aligned with the second holes; and
performing a reflow process.

[c25] 25. The method of claim 24, wherein the first carrier is a chip.

[c26] 26. The method of claim 24, wherein the first bump has a cross-sectional area larger than that of the first hole

such that the first bump engages with the first hole through the tight-fit mechanism.